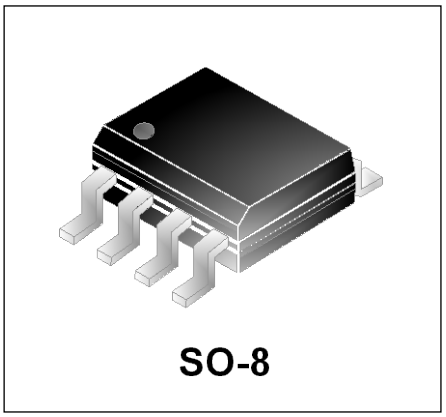
WS05-4RDA and WS12-4RDA

Transient Voltage Suppressor

Features

- Array of surge rated diodes with internal TVS diode
- Protects four I/O lines
- Low operating and clamping voltages
- Low capacitance(<15pF) for high-speed interfaces
- Solid-state technology



SO-8

IEC COMPATIBILITY (EN61000-4)

- **IEC 61000-4-2 (ESD) ±15kV (air), ±8kV (contact)**
- **IEC 61000-4-4 (EFT) 40A (5/50ns)**
- **IEC 61000-4-5 (Lightning) 24A (8/20μs)**

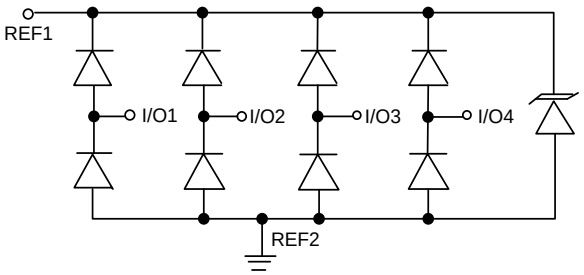
Mechanical Characteristics

- JEDEC SOIC-8 package
- Molding compound flammability rating: UL 94V-0
- Marking : Making Code
- Packaging : Tape and Reel per EIA 481
- Lead Finish: SnPb or Matte Sn

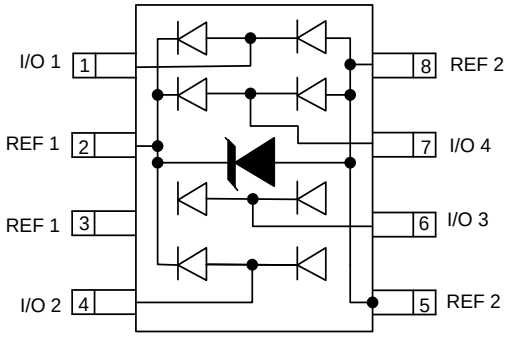
Applications

- USB Power and Data Line Protection
- T1/E1 secondary IC Side Protection
- T3/E3 secondary IC Side Protection
- HDSL, SDSL secondary IC Side Protection
- Video Line Protection
- Microcontroller Input Protection
- Base stations
- I^2C Bus Protection

Circuit diagram



Schematic and PIN Configuration



SO-8 (Top View)

Absolute Maximum Rating

Rating	Symbol	Value	Units
Peak Pulse Power (t_p=8/20μs)	P_{PP}	500	Watts
Peak Forward Voltage (I_F=1A, t_p=8/20μs)	V_{FP}	1.5	V
Lead Soldering Temperature	T_L	260(10 sec.)	°C
Operating Temperature	T_J	-55 to + 125	°C
Storage Temperature	T_{STG}	-55 to +150	°C

Electrical Characteristics

WS05-4RDA

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Reverse Stand-Off Voltage	V_{RWM}				5	V
Reverse Breakdown Voltage	V_{BR}	I_t =1mA	6			V
Reverse Leakage Current	I_R	V_{RWM}=5V,T=25°C			5	μA
Clamping Voltage	V_C	I_{PP}=1A, t_p =8/20μs			9.7	V
Clamping Voltage	V_C	I_{PP}=10A, t_p =8/20μs			12.4	V
Clamping Voltage	V_C	I_{PP}=25A, t_p =8/20μs			21	V
Peak Pulse Current	I_{PP}	t_p =8/20μs			25	A
Junction Capacitance	C_j	Between I/O pins and Ground, V_R=0V, f=1MHz		8	15	pF
		Between I/O pins V_R=0V, f=1MHz		4		pF

WS12-4RDA

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Reverse Stand-Off Voltage	V_{RWM}				12	V
Reverse Breakdown Voltage	V_{BR}	I_t =1mA	13.3			V
Reverse Leakage Current	I_R	V_{RWM}=12V,T=25°C			1	μA
Clamping Voltage	V_C	I_{PP}=1A, t_p =8/20μs			17	V
Clamping Voltage	V_C	I_{PP}=10A, t_p =8/20μs			20	V
Clamping Voltage	V_C	I_{PP}=20A, t_p =8/20μs			25	V
Peak Pulse Current	I_{PP}	t_p =8/20μs			20	A
Junction Capacitance	C_j	Between I/O pins and Ground, V_R=0V, f=1MHz		8	15	pF
		Between I/O pins V_R=0V, f=1MHz		4		pF

Typical Characteristics

Figure 1: Non-Repetitive Peak Pulse Power vs. Pulse Time

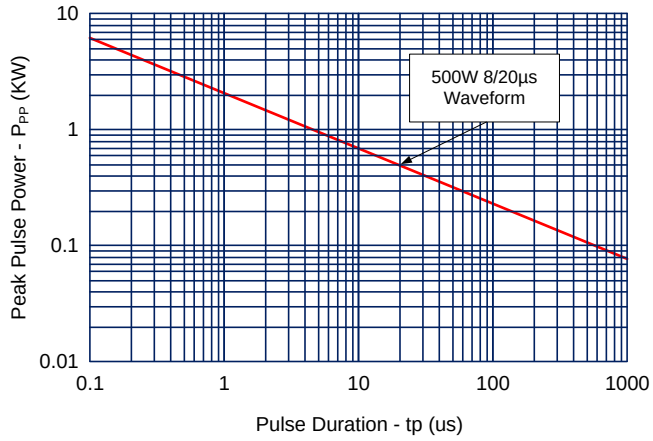


Figure 2: Power Derating Curve

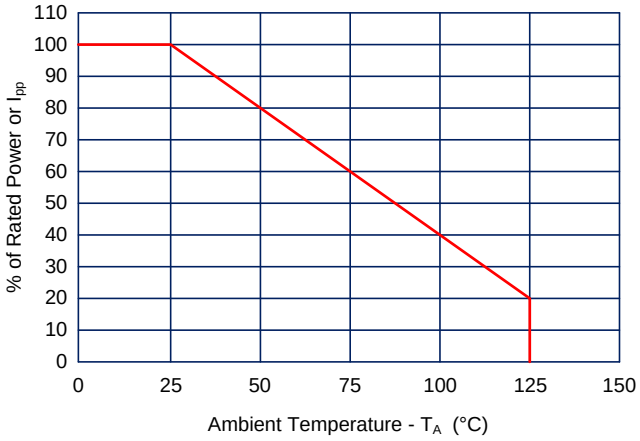


Figure 3: Pulse Waveform

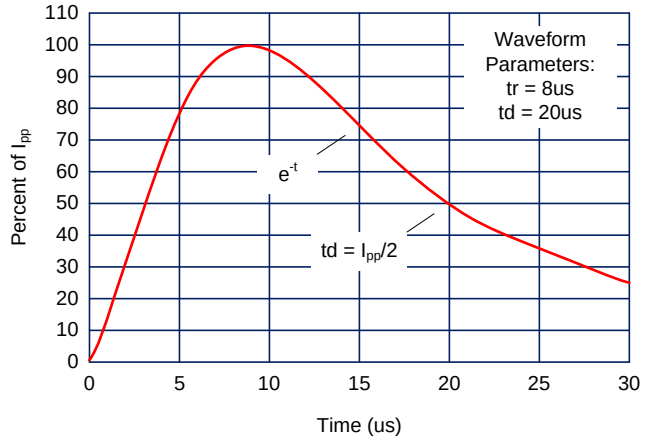


Figure 4: Clamping Voltage vs. Peak Pulse Current

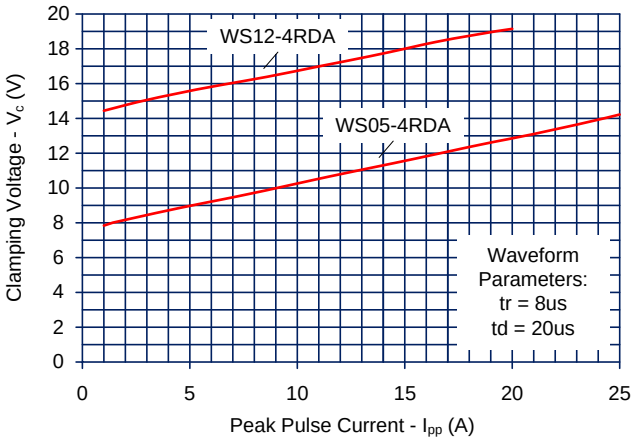


Figure 5: Variation of Capacitance vs. Reverse Voltage

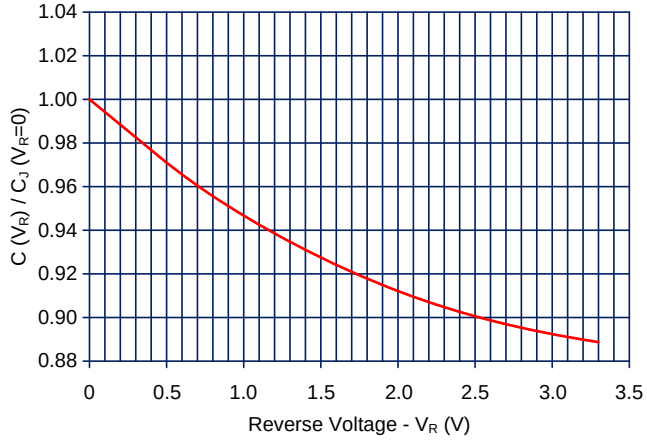
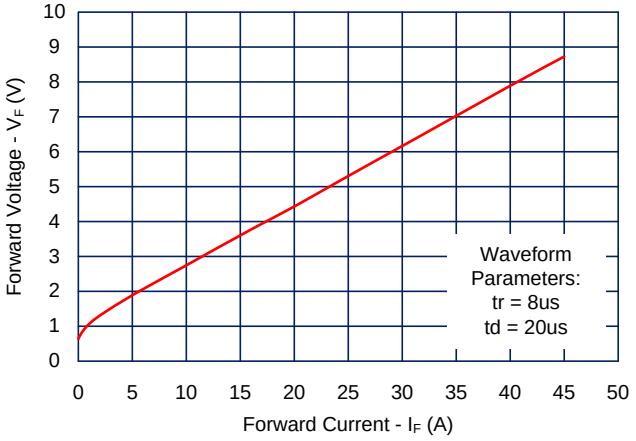


Figure 6: Forward Voltage vs. Forward Current



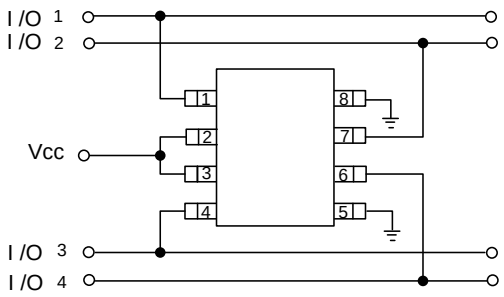
Application Information

Device Connection Options for Protection of four High-Speed Data Lines

The WSxx-4RDA TVS is designed to protect four data lines from transient over voltages by clamping them to a fixed reference. When the voltage on the protected line exceeds the reference voltage (plus diode V_F) the steering diodes are forward biased, conducting the transient current away from the sensitive circuitry. Data lines are connected at pins 1, 4, 6 and 7. The negative reference is connected at pins 5 and 8. These pins should be connected directly to a ground plane on the board for best results. The path length is kept as short as possible to minimize parasitic inductance.
The positive reference is connected at pins 2 and 3.The options for connecting the positive reference are as follows:

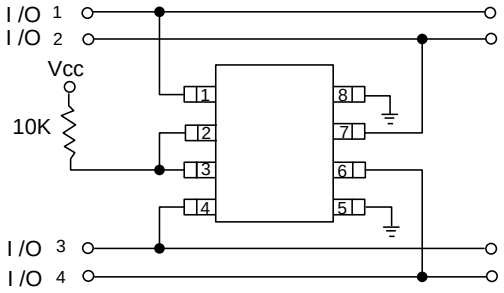
1. To protect data lines and the power line, connect pins 2 & 3 directly to the positive supply rail (V_{CC}). In this configuration the data lines are referenced to the supply voltage. The internal TVS diode prevents over-voltage on the supply rail.

Data Line and Power Supply Protection
Using Vcc as reference



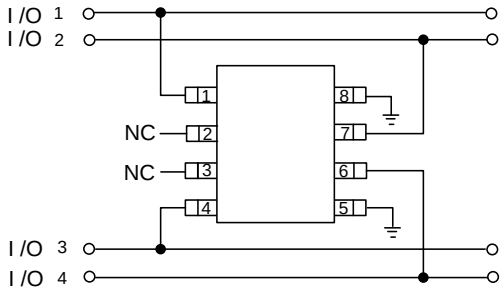
2. The WSxx-4RDA can be isolated from the power supply by adding a series resistor between pins 2 and 3 and V_{CC}. A value of 10k□ is recommended. The internal TVS and steering diodes remain biased, providing the advantage of lower capacitance.

Data Line Protection with Bias and Power
Supply Isolation Resistor

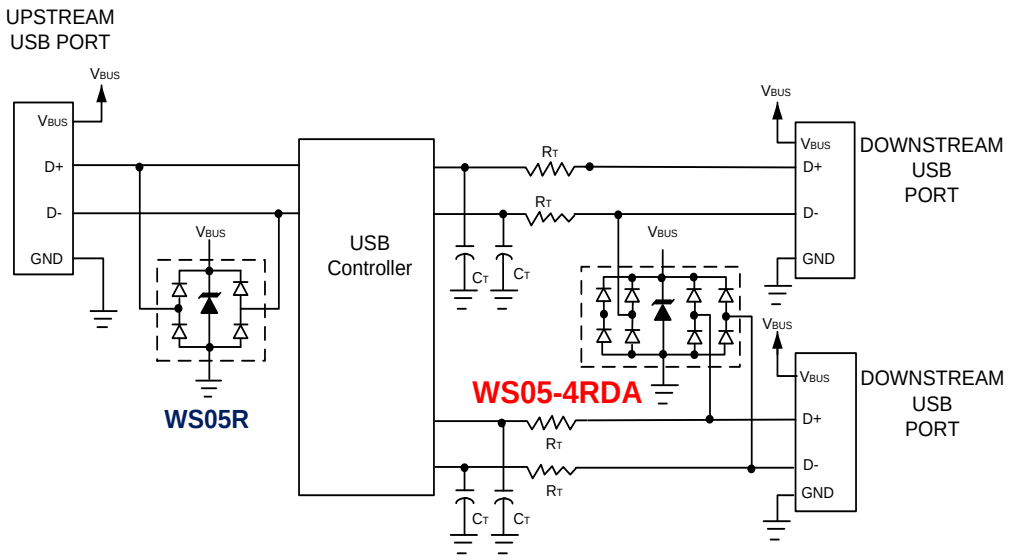


3. In applications where no positive supply reference is available, or complete supply isolation is desired, the internal TVS may be used as the reference. In this case, pins 2 and 3 are not connected. The steering diodes will begin to conduct when the voltage on the protected line exceeds the working voltage of the TVS (plus one diode drop).

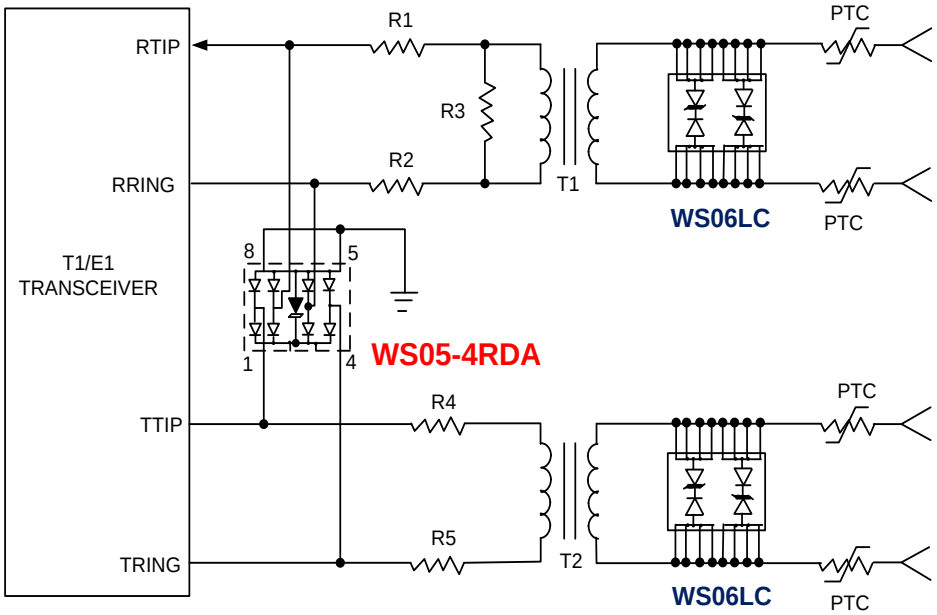
Data Line Protection Using Internal TVS
Diode as Reference



Typical Applications



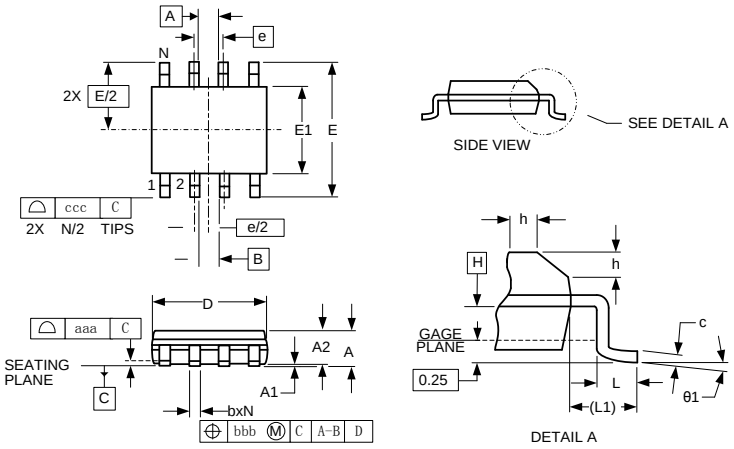
Universal Serial Bus ESD Protection



T1/E1 Interface Protection

Outline Drawing – SO-8

PACKAGE OUTLINE

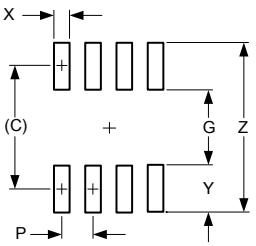


NOTES:

1. Controlling Dimensions Are In Millimeters (Angles In Degrees).
2. Datums -A- And -B- To Be Determined At Datum Plane -H-.
3. Dimensions “E1” And “D” Do Not Include Mold Flash,Protrusions Or Gate Burrs.
4. Reference JEDEC STD MS-012,VARITION AA.

SO-8

DIMENSIONS						
DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.053	-	.069	1.35	-	1.75
A1	.004	-	.010	0.10	-	0.25
A2	.049	-	.065	1.25	-	1.65
b	.012	-	.020	0.31	-	0.51
c	.007	-	.010	0.17	-	0.25
D	.189	.193	.197	4.80	4.90	5.00
E1	.150	.154	.157	3.80	3.90	4.00
E	.236BSC			6.00BSC		
e	.050 BSC			1.27 BSC		
h	.010	-	.020	0.25	-	0.50
L	.016	.028	.041	0.40	0.72	1.04
θ1	0°	-	8°	0°	-	8°
L1	(.041)			(1.04)		
N	8			8		
aaa	.004			0.10		
bbb	.010			0.25		
ccc	.008			0.20		

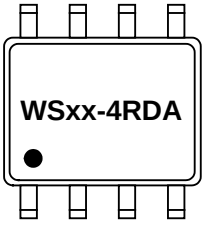


DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.205)	(5.20)
G	.118	3.00
P	.050	1.27
X	.024	0.60
Y	.087	2.20
Z	.291	7.40

Notes

1. This Land Pattern Is For Reference Purposes Only.Consult Your Manufacturing Group To Ensure Your Company's Manufacturing Guidelines Are Met.

Marking Codes



XX=Reverse Stand-Off Voltage