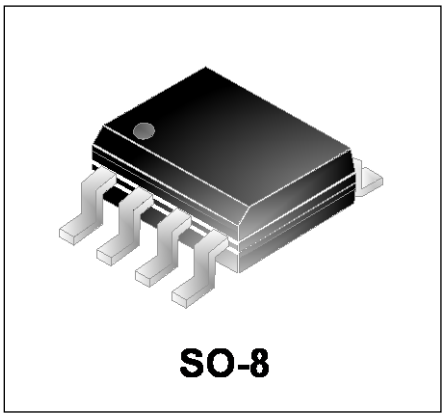
WS05-5MDAC thru WS24-5MDAC

Transient Voltage Suppressor

Features

- Transient protection for data lines
- Small SO-8 surface mount package
- Protects five I/O lines
- Working voltages: 5V, 12V, 15V and 24V
- Low leakage current
- Low operating and clamping voltages
- Solid-state silicon avalanche technology



IEC COMPATIBILITY (EN61000-4)

- **IEC 61000-4-2 (ESD) ±15kV (air), ±8kV (contact)**
- **IEC 61000-4-4 (EFT) 40A (5/50ns)**
- **IEC 61000-4-5 (Lightning) 12A (8/20μs)**

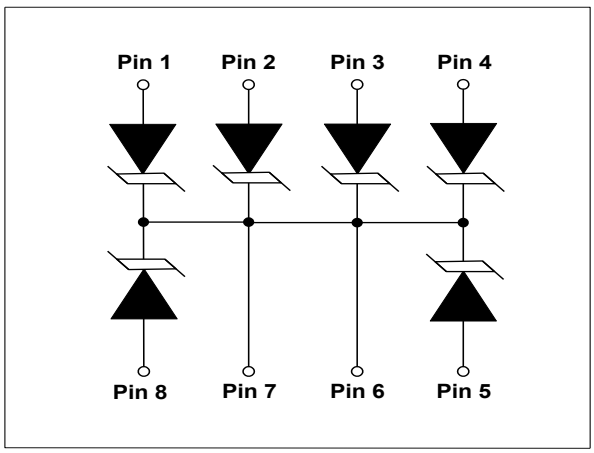
Mechanical Characteristics

- JEDEC SO-8 package
- Molding compound flammability rating: UL 94V-0
- Marking: Part number, date code, logo
- Packaging: Tube or Tape and Reel per EIA 481

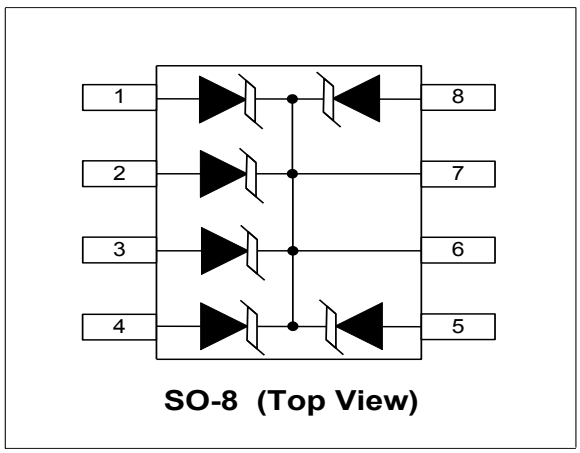
Applications

- RS-232 and RS-422 Data Lines
- Microprocessor based equipment
- LAN/WAN equipment
- Notebook ,Desktops, and Servers
- Instrumentation
- Peripherals
- Serial and Parallel Ports

Circuit Diagram (Each Line Pair)



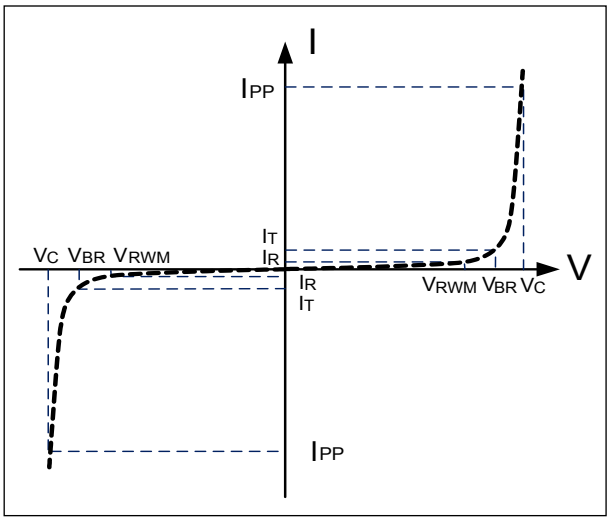
Schematic & PIN Configuration



Absolute Maximum Rating			
Rating	**Symbol**	**Value**	**Units**
Peak Pulse Power (t_p =8/20μs)	P_{PK}	300	Watts
Lead Soldering Temperature	T_L	260 (10 sec.)	℃
Operating Temperature	T_J	-55 to + 125	℃
Storage Temperature	T_{STG}	-55 to +150	℃

Electrical Parameters (T=25℃)

Symbol	Parameter
I_{PP}	Maximum Reverse Peak Pulse Current
V_C	Clamping Voltage @ I_{PP}
V_{RWM}	Working Peak Reverse Voltage
I_R	Maximum Reverse Leakage Current @ V_{RWM}
V_{BR}	Breakdown Voltage @ I_T
I_T	Test Current
I_F	Forward Current
V_F	Forward Voltage @ I_F



Electrical Characteristics

WS05-5MDAC						
Parameter	**Symbol**	**Conditions**	**Min**	**Typical**	**Max**	**Units**
Reverse Stand-Off Voltage	V_{RWM}				5.0	V
Reverse Breakdown Voltage	V_{BR}	I_T=1mA	6.0			V
Reverse Leakage Current	I_R	V_{RWM}=5V,T=25℃			20	μA
Clamping Voltage	V_C	I_{PP}=1A, t_p=8/20μs			9.8	V
Maximum Peak Pulse Current	I_{PP}	t_p=8/20μs			17	A
Junction Capacitance	C_j	V_R = 0V, f = 1MHz			350	pF

Electrical Characteristics (Continued)

WS12-5MDAC						
Parameter	**Symbol**	**Conditions**	**Min**	**Typical**	**Max**	**Units**
Reverse Stand-Off Voltage	V_{RWM}				12	V
Reverse Breakdown Voltage	V_{BR}	I_T=1mA	16.7			V
Reverse Leakage Current	I_R	V_{RWM}=5V,T=25℃			1	μA
Clamping Voltage	V_C	I_{PP}=1A, t_p=8/20μs			19	V
Maximum Peak Pulse Current	I_{PP}	t_p=8/20μs			12	A
Junction Capacitance	C_j	V_R = 0V, f = 1MHz			120	pF

WS15-5MDAC						
Parameter	**Symbol**	**Conditions**	**Min**	**Typical**	**Max**	**Units**
Reverse Stand-Off Voltage	V_{RWM}				15	V
Reverse Breakdown Voltage	V_{BR}	I_T=1mA	16.7			V
Reverse Leakage Current	I_R	V_{RWM}=5V,T=25℃			1	μA
Clamping Voltage	V_C	I_{PP}=1A, t_p=8/20μs			24	V
Maximum Peak Pulse Current	I_{PP}	t_p=8/20μs			10	A
Junction Capacitance	C_j	V_R = 0V, f = 1MHz			75	pF

WS24-5MDAC						
Parameter	**Symbol**	**Conditions**	**Min**	**Typical**	**Max**	**Units**
Reverse Stand-Off Voltage	V_{RWM}				24	V
Reverse Breakdown Voltage	V_{BR}	I_T=1mA	26.7			V
Reverse Leakage Current	I_R	V_{RWM}=5V,T=25℃			1	μA
Clamping Voltage	V_C	I_{PP}=1A, t_p=8/20μs			43	V
Maximum Peak Pulse Current	I_{PP}	t_p=8/20μs			5	A
Junction Capacitance	C_j	V_R = 0V, f = 1MHz			50	pF

Typical Characteristics

Figure 1: Non Repetitive Peak Pulse Power vs. Pulse Time

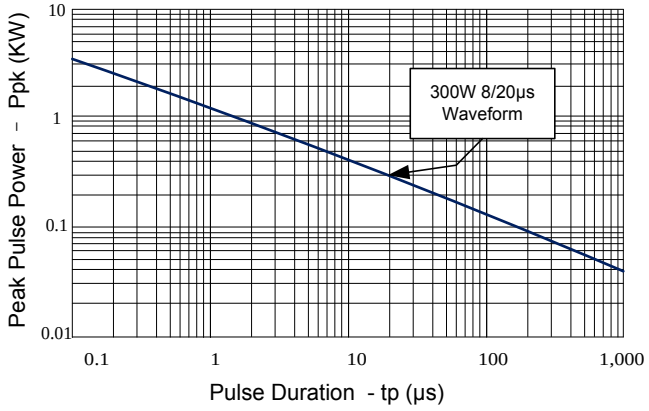


Figure 2: Power Derating Curve

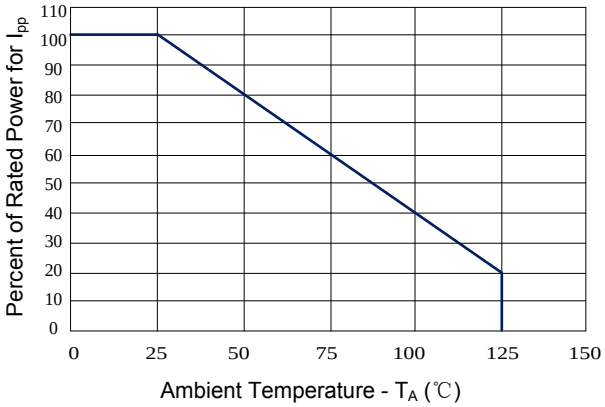


Figure 3: Pulse Waveform

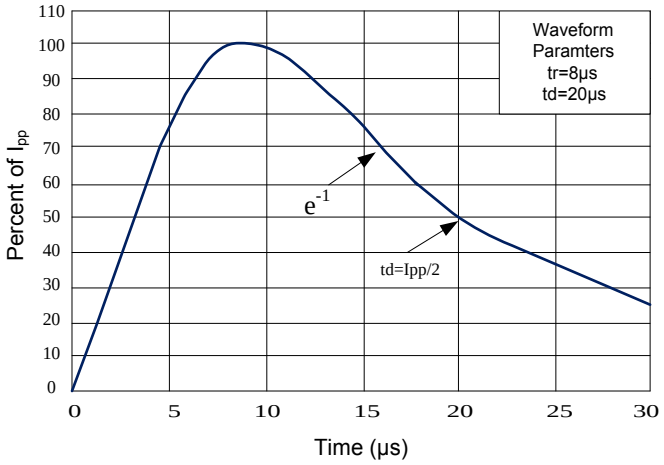


Figure 4: ESD Pulse Waveform (IEC 61000-4-2)

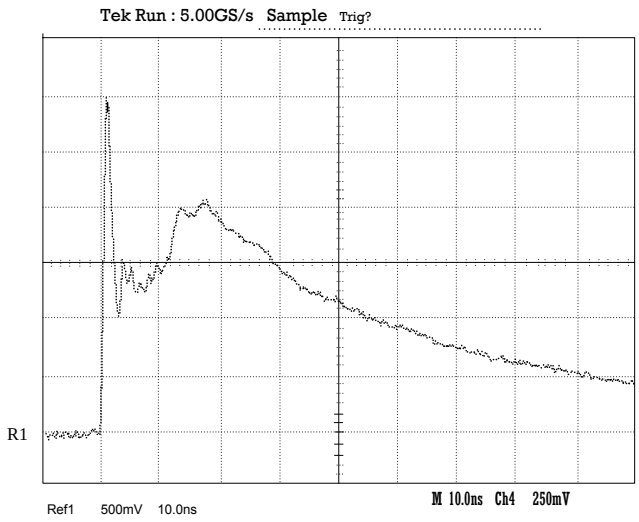


Figure 5: ESD Discharge Parameters Per IEC 61000-4-2

Level	First Peak Current (A)	Peak Current at 30ns (A)	Peak Current at 60ns (A)	Test Voltage (Contact Discharge) (kV)	Test Voltage (Air Discharge) (kV)
1	7.5	4	8	2	2
2	15	8	4	4	4
3	22.5	12	6	6	8
4	30	16	8	8	15

Applications Information

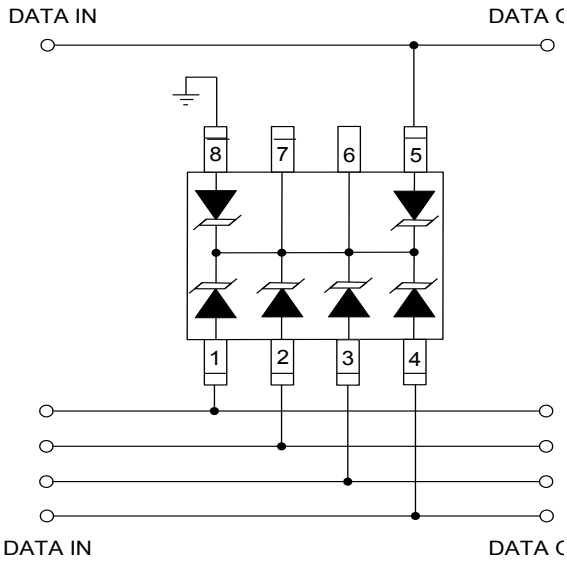
Device Connection for Protection of Five Data Lines

The WSxx-5MDAC is designed to protect up to 5 data or I/O lines. They are bidirectional devices and may be used on lines where the signal polarities are above and below ground.

The WSxx-5MDAC TVS arrays employ a monolithic structure. Therefore, the working voltage (V_{RWM}) and breakdown voltage (V_{BR}) specifications apply to the differential voltage between any two data line pins. For example, the SMDA24C-5 is designed for a maximum voltage excursion of ±12V between any two data lines. The device is connected as follows:

Pins 1, 2, 3, 4, and 5 are connected to the lines that are to be protected. Pin 8 is connected to ground. The ground connections should be made directly to the ground plane for best results. The path length is kept as short as possible to reduce the effects of parasitic inductance in the board traces. Pins 6 and 7 are not connected.

Connection Diagram



Circuit Board Layout Recommendations for Suppression of ESD

Good circuit board layout is critical for the suppression of ESD induced transients. The following guidelines are recommended:

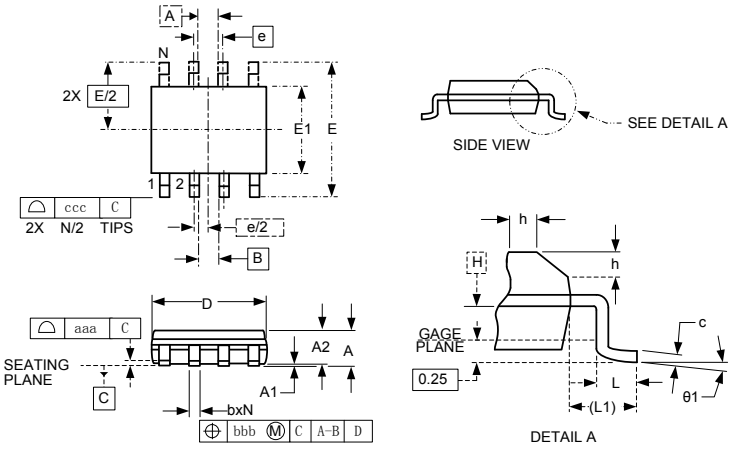
- Place the TVS near the input terminals or connectors to restrict transient coupling.
- Minimize the path length between the TVS and the protected line.
- Minimize all conductive loops including power and ground loops.
- The ESD transient return path to ground should be kept as short as possible.
- Never run critical signals near board edges.
- Use ground planes whenever possible.

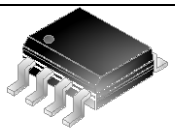
Matte Tin Lead Finish

Matte tin has become the industry standard lead-free replacement for SnPb lead finishes. A matte tin finish is composed of 100% tin solder with large grains. Since the solder volume on the leads is small compared to the solder paste volume that is placed on the land pattern of the PCB, the reflow profile will be determined by the requirements of the solder paste. Therefore, these devices are compatible with both lead-free and SnPb assembly techniques. In addition, unlike other lead-free compositions, matte tin does not have any added alloys that can cause degradation of the solder joint.

Outline Drawing – SO-8

PACKAGE OUTLINE



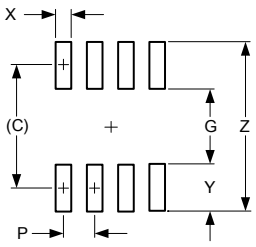


SO-8

NOTES:

1. Controlling Dimensions Are In Millimeters (Angles In Degrees).
2. Datums -A- And -B- To Be Determined At Datum Plane -H-.
3. Dimensions “E1” And “D” Do Not Include Mold Flash,Protrusions Or Gate Burrs.
4. Reference JEDEC STD MS-012,VARITION AA.

DIMENSIONS						
DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.053	-	.069	1.35	-	1.75
A1	.004	-	.010	0.10	-	0.25
A2	.049	-	.065	1.25	-	1.65
b	.012	-	.020	0.31	-	0.51
c	.007	-	.010	0.17	-	0.25
D	.189	.193	.197	4.80	4.90	5.00
E1	.150	.154	.157	3.80	3.90	4.00
E	.236BSC			6.00BSC		
e	.050 BSC			1.27 BSC		
h	.010	-	.020	0.25	-	0.50
L	.016	.028	.041	0.40	0.72	1.04
θ1	0°	-	8°	0°	-	8°
L1	(.041)			(1.04)		
N	8			8		
aaa	.004			0.10		
bbb	.010			0.25		
ccc	.008			0.20		

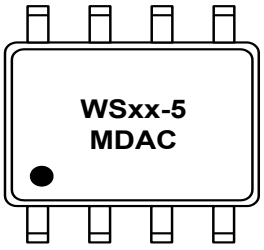


DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.205)	(5.20)
G	.118	3.00
P	.050	1.27
X	.024	0.60
Y	.087	2.20
Z	.291	7.40

Notes

1. This Land Pattern Is For Reference Purposes Only. Consult Your Manufacturing Group To Ensure Your Company's Manufacturing Guidelines Are Met.

Marking Codes



XX=Reverse Stand-Off Voltage