

WS05-7MDA Thru WS24-7MDA

Transient Voltage Suppressor

Document: W0301045, Rev: A

Features

- Transient protection for data lines to
- Protects seven I/O lines
- Small SO-8 surface mount package
- Working voltages: 5V, 12V, 15V and 24V
- Low leakage current
- Low operating and clamping voltages
- Solid-state silicon avalanche technology

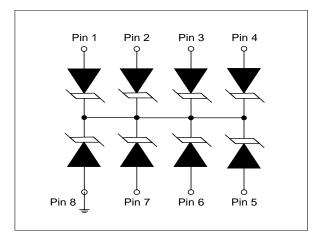
IEC COMPATIBILITY (EN61000-4)

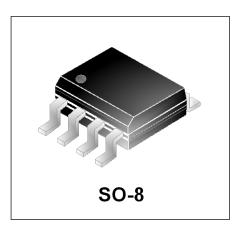
- IEC 61000-4-2 (ESD) ±15kV (air), ±8kV (contact)
- IEC 61000-4-4 (EFT) 40A (5/50ns)
- IEC 61000-4-5 (Lightning) 12A (8/20µs)

Mechanical Characteristics

- JEDEC SO-8 package
- Molding compound flammability rating: UL 94V-0
- Marking: Part number, date code, logo
- Packaging:Tube or Tape and Reel per EIA 481
- RoHS Compliant

Circuit Diagram (Each Line Pair)

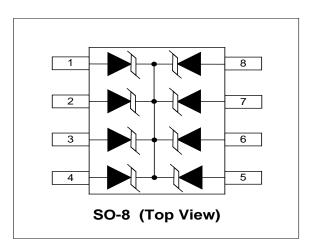




Applications

- RS-232 and RS-422 Data Lines
- LAN/WAN Equipment
- Notebooks, Desktops, and Servers
- Instrumentation
- Peripherals
- Set Top Box
- Serial and Parallel Port

Schematic & PIN Configuration

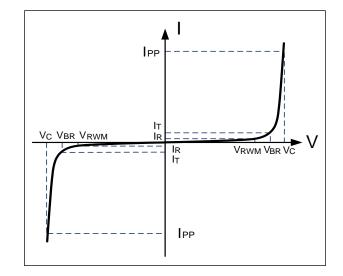


Silicontrol[™] Overvoltage Protection Products

| Absolute Maximum Rating | | | | | |
|---|------------------|---------------|-------|--|--|
| Rating | Symbol | Value | Units | | |
| Peak Pulse Power ($t_p = 8/20 \mu s$) | Р _{РК} | 300 | Watts | | |
| Lead Soldering Temperature | TL | 260 (10 sec.) | °C | | |
| Operating Temperature | TJ | -55 to + 125 | °C | | |
| Storage Temperature | T _{STG} | -55 to +150 | ° | | |

Electrical Parameters (T=25°C)

| Symbol | Parameter | | | |
|--------|--|--|--|--|
| Ірр | Maximum Reverse Peak Pulse Current | | | |
| Vc | Clamping Voltage @ IPP | | | |
| VRWM | Working Peak Reverse Voltage | | | |
| IR | Maximum Reverse Leakage Current @ VRWM | | | |
| Vbr | Breakdown Voltage @ I⊤ | | | |
| Iτ | Test Current | | | |
| lF | Forward Current | | | |
| VF | Forward Voltage @ I⊧ | | | |



Electrical Characteristics

| WS05-7MDA | | | | | | |
|---------------------------|------------------|---|-----|---------|-----|-------|
| Parameter | Symbol | Conditions | Min | Typical | Мах | Units |
| Reverse Stand-Off Voltage | V _{RWM} | | | | 5.0 | V |
| Reverse Breakdown Voltage | V _{BR} | I _T =1mA | 6.0 | | | V |
| Reverse Leakage Current | I _R | V _{RWM} =5V,T=25°C | | | 20 | μA |
| Clamping Voltage | Vc | I _{PP} =1A, t _p =8/20µs | | | 9.9 | V |
| Maximum PeakPulse Current | I _{PP} | t _p =8/20μs | | | 17 | А |
| Junction Capacitance | Cj | Between I/O Pins and Ground V _R = 0V, f = 1MHz | | | 350 | pF |

∠ Silicontrol[™] Overvoltage Protection Products

Electrical Characteristics(Cont.)

| WS12-7MDA | | | | | | |
|---------------------------|------------------|---|--------|---------|-----|-------|
| Parameter | Symbol | Conditions | Min | Typical | Max | Units |
| Reverse Stand-Off Voltage | V _{RWM} | | | | 12 | V |
| Reverse Breakdown Voltage | V _{BR} | I _T =1mA | 13.3 | | | V |
| Reverse Leakage Current | I _R | V _{RWM} =5V,T=25°C | | | 1 | μA |
| Clamping Voltage | Vc | I _{PP} =1A, t _p =8/20μs | | | 19 | V |
| Maximum PeakPulse Current | I _{PP} | t _p =8/20μs | | | 12 | А |
| Junction Capacitance | Cj | Between I/O Pins and Ground V _R = 0V, f = 1MHz | Ground | | 120 | pF |
| WS15-7MDA | | | | | | |
| Parameter | Symbol | Conditions | Min | Typical | Max | Units |
| Reverse Stand-Off Voltage | V _{RWM} | | | | 15 | V |
| Reverse Breakdown Voltage | V _{BR} | I _T =1mA | 16.7 | | | V |
| Reverse Leakage Current | I _R | V _{RWM} =5V,T=25°C | | | 1 | μA |
| Clamping Voltage | Vc | I _{PP} =1A, t _p =8/20μs | | | 24 | V |
| Maximum PeakPulse Current | I _{PP} | t _p =8/20μs | | | 10 | А |
| Junction Capacitance | Cj | Between I/O Pins and Ground V _R = 0V, f = 1MHz | | | 75 | pF |
| WS24-7MDA | | | | | | |
| Parameter | Symbol | Conditions | Min | Typical | Max | Units |
| Reverse Stand-Off Voltage | V _{RWM} | | | | 24 | V |
| Reverse Breakdown Voltage | V _{BR} | I _T =1mA | 26.7 | | | V |
| Reverse Leakage Current | I _R | V _{RWM} =5V,T=25°C | | | 1 | μA |
| Clamping Voltage | Vc | I _{PP} =1A, t _p =8/20µs | | | 43 | V |
| Maximum PeakPulse Current | I _{PP} | t _p =8/20µs | | | 5 | А |
| Junction Capacitance | Cj | Between I/O Pins and Ground V _R = 0V, f = 1MHz | | | 50 | pF |

WSxx-7MDA

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Typical Characteristics

10

1

0.1

0.01

0.1

Peak Pulse Power - Ppk (KW)

Figure 1: Non Repetitive Peak Pulse Power vs. Pulse Time

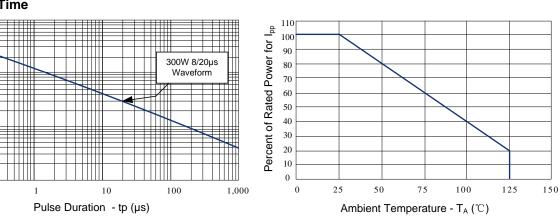
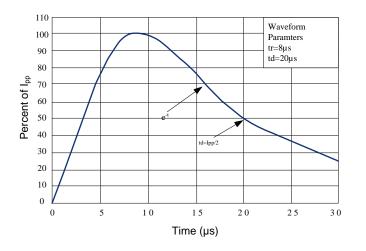


Figure 3: Pulse Waveform





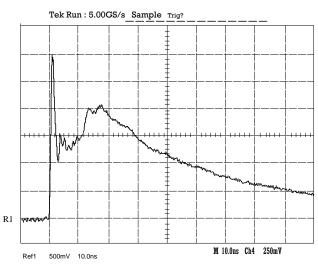


Figure 5: ESD Discharge Parameters Per IEC 61000-4-2

Figure 2: Power Derating Curve

| Level | First Peak Current (A) | Peak Current at 30ns (A) | Peak Current at 60ns (A) | Test Voltage (Contact Discharge) (kV) | Test Voltage (Air Discharge) (kV) |
|-------|---------------------------------|-----------------------------------|-----------------------------------|---|---|
| 1 | 7.5 | 4 | 8 | 2 | 2 |
| 2 | 15 | 8 | 4 | 4 | 4 |
| 3 | 22.5 | 12 | 6 | 6 | 8 |
| 4 | 30 | 16 | 8 | 8 | 15 |

Applications Information

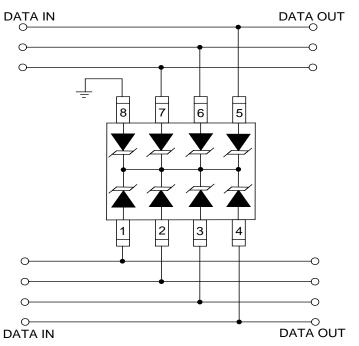
Device Connection for Protection of Seven Data Lines

The Wxx-7MDA is designed to protect up to 7 data or I/O lines. They are bidirectional devices and may be used on lines where the signal polarities are above and below ground.

The Wxx-7MDA TVS arrays employ a monolithic structure. Therefore, the working voltage (V_{RWM}) and breakdown voltage (V_{BR}) specifications apply to the differential voltage between any two data line pins. For example, the W12-7MDA is designed for a maximum voltage excursion of ±6V between any two data lines.

The device is connected as follows:

Pins 1, 2, 3, 4, 5, 6 and 7 are connected to the lines that are to be protected. Pin 8 is connected to ground. The ground connections should be made directly to the ground plane for best results. The path length is kept as short as possible to reduce the effects of parasitic inductance in the board traces.



Connection Diagram

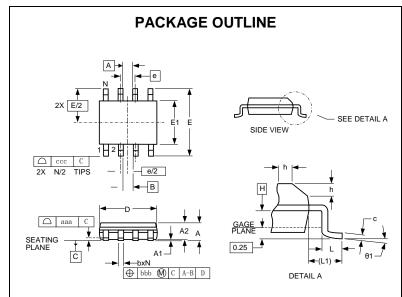
Circuit Board Layout Recommendations for Suppression of ESD.

Good circuit board layout is critical for the suppression of ESD induced transients. The following guidelines are recommended:

- Place the TVS near the input terminals or connectors to restrict transient coupling.
- Minimize the path length between the TVS and the protected line.
- Minimize all conductive loops including power and ground loops.
- The ESD transient return path to ground should be kept as short as possible.
- Never run critical signals near board edges.
- Use ground planes whenever possible.

WSxx-7MDA

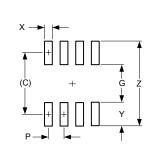
Outline Drawing – SO-8



| JT ST | | | | | | | |
|-------|---------|----------|---------|----------|-------------|------|--|
| | | | SO-8 | 3 | | | |
| | I | 0 | DIMENSI | ONS | | | |
| DIM | | INCHES | 1 | N | MILLIMETERS | | |
| Dim | MIN | NOM | MAX | MIN | NOM | MAX | |
| А | .053 | - | .069 | 1.35 | - | 1.75 | |
| A1 | .004 | - | .010 | 0.10 | - | 0.25 | |
| A2 | .049 | - | .065 | 1.25 | - | 1.65 | |
| b | .012 | - | .020 | 0.31 | - | 0.51 | |
| С | .007 | - | .010 | 0.17 | - | 0.25 | |
| D | .189 | .193 | .197 | 4.80 | 4.90 | 5.00 | |
| E1 | .150 | .154 | .157 | 3.80 | 3.90 | 4.00 | |
| Е | .236BSC | | | 6.00BSC | | | |
| е | | .050 BSC | ; | 1.27 BSC | | | |
| h | .010 | - | .020 | 0.25 | - | 0.50 | |
| L | .016 | .028 | .041 | 0.40 | 0.72 | 1.04 | |
| θ1 | 0° | - | 8° | 0° | - | 8° | |
| L1 | (.041) | | | (1.04) | | | |
| Ν | 8 | | | 8 | | | |
| aaa | .004 | | | 0.10 | | | |
| bbb | .010 | | | 0.25 | | | |
| ссс | .008 | | | | 0.20 | | |

NOTES:

- 1. Controlling Dimensions Are In Millimeters (Angles In Degrees).
- 2. Datums And B- To Be Determined At Datum Plane H-.
- 3. Dimensions "E1" And "D" Do Not Include Mold Flash, Protrusions Or Gate Burrs.
- 4. Reference JEDEC STD MS-012, VARITION AA.



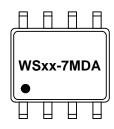
| DIMENSIONS | | | | |
|------------|--------------------|--------|--|--|
| DIM | INCHES MILLIMETERS | | | |
| С | (.205) | (5.20) | | |
| G | .118 | 3.00 | | |
| Р | .050 | 1.27 | | |
| х | .024 | 0.60 | | |
| Y | .087 | 2.20 | | |
| z | .291 | 7.40 | | |

Notes

1.

This Land Pattern Is For Reference Purposes Only.Consult Your Manufacturing Group To Ensure Your Company's Manufacturing Guidelines Are Met.

Marking Codes



XX=Reverse Stand-Off Voltage

